Abstract

A stress migration test structure is provided that can be used to detect stress migration defects in traces or conductors of integrated circuits. The stress migration test structure can be placed between die areas on a wafer, or on a die. On the die, a stress migration test structure can be placed in otherwise unused areas of a die such as between bond pads and the periphery of a die, in a layer beneath bond pads, in a region between the bond pads and the perimeter of standard area for circuit layout, or in regions in more than one level of the integrated circuit. The stress migration test structure may also be placed within the standard area for circuit layout and used, with some additional circuitry, as a stress migration test structure on an integrated circuit once the die is packaged. Obtaining information from the impedance segments of a stress migration test structure can be accomplished employing either a mechanical stepping or an electrical stepping technique.